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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,312	06/24/2003	Kenneth W. Marr	303.859US1	8022

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
SIDDIQUI, SAQIB JAVAID	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,312	MARR, KENNETH W.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-16 and 48-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-77* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12 are, drawn to a device for repairing defects in a circuit, classified in class 714, subclass 718.

II. Claims 13-16, 48-62, & 63-65 are, drawn to a device, system, and method of testing an integrated circuit and repairing the memory using redundant memory, classified in class 714, subclass 710.

III. Claims 17-47, & 66-75 are drawn to different embodiments of groups II, & I classified in class 714, subclass 718.

Inventions I, II and III are related as products which share a disclosed common utility linked to a substantial structural feature. The products in this relationship are distinct if either or both of the following can be shown: (1) that the products encompass embodiments that are NOT required to perform the common utility or (2) that the products as claimed encompass embodiments that are NOT required to have the substantial structural feature. In this case, the embodiments described in group II are sufficient to perform the functions of the invention. The embodiments taught by claims in groups I and III are not required to perform the common utility.

Inventions I, II and III are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and

(2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because II does not require the exact embodiments as provided in groups I and II. The subcombination has separate utility such as testing memory.

Because these inventions are independent or distinct for the reasons given above and the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

During a telephone conversation with Viet Tong on 06/15/06 a provisional election was made without traverse to prosecute the invention of II, claims 13-16, 48-62, & 63-65. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-12, 17-47, & 66-75 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Oath/Declaration

The Oath filed June 24, 2003 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 13-16, & 48-65 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Namekawa US Pat no. 6,115,301.

As per claims 13:

Namekawa substantially teaches a device comprising: a first supply node and a second supply node (column 7, lines 3-20); a plurality of memory segments connected in parallel with each other (Figure 1 # 10); a plurality of switching units, each of the switching units connecting in series with one of the memory segments between the second supply node and one of the internal nodes (column 3, lines 23-50), wherein each of the switching units includes an input node for receiving a select signal to electrically disconnect one of the memory segments from the second supply node based on a state of the select signal (Figure 1 # 70, column 6, lines 5-30); and a redundant array for replacing at least one memory segment of the plurality of memory segments (Figure 1 # 20).

Namekawa discloses the claimed invention except for the exact location of the switching units. It would have been obvious to one having ordinary skill in the art at the time the invention was made to place the switching units between the second supply nods and one of the internal nodes, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

As per claim 14:

Namekawa teaches the device as rejected in claim 13 above, further comprising a redundancy controller connected to the switching units for selectively setting the state of the select signal based on a number of programming signals (column 4, lines 25-50).

As per claim 15:

Namekawa teaches the device as rejected in claim 14 above, further comprising a programming unit for generating the programming signals based on a programmed address stored in the programming unit (column 7, lines 20-40).

As per claim 16:

Namekawa teaches the device as rejected in claim 13 above, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least one of the memory groups of at least one of the memory segments is defective (Figure 1 # 10).

As per claim 48:

Namekawa substantially teaches a device comprising: a first supply node and a second supply node (column 7, lines 3-20); a plurality of memory segments, each of the memory segments including a plurality of memory cells (Figure 1 # 10), each of the memory cells including: a first storage node and a second storage node (Figure 2 # 80); a latch connected to the first and second storage node and connected in between a first internal node and a second internal node (column 1, lines 5-40); a first access element for accessing the first storage node; and a second access element for accessing the second storage node column 6, lines 25-50); a plurality of first switching units, each of the first switching units connecting in between the first supply node and one of the memory segments (column 3, lines 23-50); and a plurality of second switching units, each of the second switching units connecting between the second supply node and one of the memory segments (Figure 1 # 70, column 6, lines 5-30).

Namekawa discloses the claimed invention except for the exact location of the switching units. It would have been obvious to one having ordinary skill in the art at the time the invention was made to place the switching units between the second supply nods and one of the internal nodes, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

As per claim 49:

Namekawa teaches the device as rejected in claim 48 above, wherein at least one of the memory segments is defective (column 3, lines 25-50).

As per claim 50:

Namekawa teaches the device as rejected in claim 48 above, wherein at least one of the memory segments has a circuit short between the first and second internal nodes (column 4, lines 30-50).

As per claim 51:

Namekawa teaches the device as rejected in claim 48 above, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least one of the memory groups of at least one of the memory segments is defective (Figure 1 # 10).

As per claim 52:

Namekawa teaches the device as rejected in claim 48 above, wherein in each of the memory segments, the plurality of memory cells are arranged in a plurality of rows connected in parallel between one of the first switching unit and one of the second switching units (Figure 1 # 40).

As per claim 53:

Namekawa teaches the device as rejected in claim 48 above, wherein each of the first switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments (column 5, lines 37-50).

As per claim 54:

Namekawa teaches the device as rejected in claim 48 above, wherein each of the second switching units includes a transistor having a source and a drain connected between the second supply node and one of the memory segments (column 5, lines 37-50).

As per claim 55:

Namekawa teaches the device as rejected in claim 48 above, wherein the latch includes: a first inverter having an input node connected to the first storage node and an output node connected to the second storage node; and a second inverter having an input node connected to the second storage node and an output node connected to the first storage node (column 8, lines 25-40).

As per claims 56:

Namekawa teaches the device as rejected in claim 55 above, wherein one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line (column 5, lines 37-50).

As per claim 57:

Namekawa teaches the device as rejected in claim 56 above, herein the latch includes: a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node; and a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node (column 5, lines 37-50).

As per claims 58-62:

Claims 58-62 are directed to a system of claims 13-16 & 48-57. Namekawa teaches as stated above, the device as set forth in claims 13-16 & 48-57. Therefore, Namekawa also teaches, as stated above, the system as set forth in claims 58-62.

As per claims 63-65:

Claims 63-65 are directed to a method of claims 13-16 & 48-57. Namekawa teaches as stated above, the device as set forth in claims 13-16 & 48-57. Therefore, Namekawa also teaches, as stated above, the method as set forth in claims 63-65.

Claims 13, 48, 58, & 63 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Cleveland et al. US Pat no. 5,349,558.

Cleveland et al. substantially teaches a device, method and a system comprising a processor (Figure 1); and a memory device connected to the processor, the memory device including (Figure 1): a supply node for providing a voltage source (Figure 1 "VCC); a memory array connected to the supply node via a supply path for receiving the voltage source (Figure 1); a supply control circuit connected in the supply path for isolating a memory segment of the memory array from the supply node if the memory

segment is defective (column 4, lines 45-66); and a redundant array for replacing the memory segment if the memory segment is defective (Figure 1 # 6).

Cleveland et al. discloses the claimed invention except that it uses the transistor instead of the supply control circuit. The reference demonstrates that the transistor is an equivalent structure known in the art. Therefore, because these two were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the transistor for the supply control circuit.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. (5795797 A, 6249465 B, and 5907515 A) mention the same redundant scheme with defect isolation are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

Saqib Siddiqui
Art Unit 2138
06/20/2006

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100